

WHAT IS CLAIMED IS

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1. A probe card for testing a semiconductor chip, comprising:

a plurality of probes;

a build-up interconnection layer having a
10 multilayer interconnection structure therein, said
build-up interconnection layer carrying said plurality
of probes on a top surface thereof in electrical
connection with said multilayer interconnection
structure; and

15 a capacitor embedded in a resin insulation
layer constituting said build-up interconnection layer
in electrical connection with one of said probes via
said multilayer interconnection structure,

said multilayer interconnection structure
20 including an inner via-contact in the vicinity of said
probe.

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2. A probe card as claimed in claim 1,
wherein said capacitor has a thickness generally equal
to or less than a thickness of said resin insulation
layer.

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3. A probe card as claimed in claim 1,
35 wherein said capacitor is formed on a silicon
substrate having a polished bottom surface and
includes a structure sandwiching a dielectric film by

upper and lower electrode films, said structure being formed on a top surface of said silicon substrate.

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4. A probe card as claimed in claim 1, wherein said capacitor is formed in said build-up interconnection layer, right underneath one of said probes.

15 5. A probe card as claimed in claim 1, wherein said probe card includes therein a plurality of said capacitors, said capacitors being connected to respective power lines of different supply voltages.

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6. A probe card as claimed in claim 1, wherein said capacitor includes a dielectric film of a complex oxide containing at least one metal element selected from the group consisting of Sr, Ba, Pb, Zr, Bi, Ta, Ti, Mg and Nb.

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7. A probe card as claimed in claim 1, wherein said capacitor includes an upper and lower electrodes sandwiching a dielectric film, said first and second electrodes containing at least one metal element or a metal oxide selected from the group consisting of Pt, Au, Cu, Pb, Ru, a Ru oxide, Ir, an

Ir oxide, and Cr.

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8. A probe card as claimed in claim 1,
wherein said capacitor has a thickness of $30\mu\text{m}$ or
less, said thickness including a thickness of a
support substrate on which said capacitor is formed
10 and a height of a terminal electrode.

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9. A probe card as claimed in claim 1,
wherein said capacitor is a thin-film capacitor formed
on a support substrate and has a laminated structure
formed on said support substrate, said laminated
structure including a dielectric film sandwiched by
20 upper and lower electrode films.

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10. A testing method of a semiconductor
device by using a probe card,
said probe card comprising: a plurality of
probes; a build-up interconnection layer having a
multilayer interconnection structure therein, said
30 build-up interconnection layer carrying said plurality
of probes on a top surface thereof in electrical
connection with said multilayer interconnection
structure; and a capacitor embedded in a resin
insulation layer constituting said build-up
35 interconnection layer in electrical connection with
one of said probes via said multilayer interconnection
structure, said multilayer interconnection structure

including an inner via-contact in the vicinity of said probe,

said method comprising the steps of:

causing said probe card to make a contact
5 with a semiconductor chip to be tested such that said semiconductor chip is in electrical connection with said probe card; and

testing electric properties of said semiconductor chip,

10 said method further comprising the step, before contacting said probe card to said semiconductor chip, of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package
15 including therein said semiconductor chip and a capacitor, for a part between said semiconductor chip and said capacitor.

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11. A testing method as claimed in claim 10, wherein said test is conducted in the state said semiconductor chip forms a semiconductor wafer.

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12. A probe card for testing a semiconductor
30 chip, comprising:

a first interconnection substrate;

a second interconnection substrate mounted on said first interconnection board in such a manner that a gap is formed between said first
35 interconnection substrate and said second interconnection substrate;

a plurality of probes provided on said

second interconnection substrate at a surface away
from said first interconnection substrate; and
a decoupling capacitor provided on said
second interconnection substrate at a surface facing
5 said first interconnection substrate.

10 13. A probe card as claimed in claim 12,
wherein said first interconnection substrate includes
therein an interconnection structure including an
inner via-contact, said second interconnection
substrate having a thickness of 1mm or less.

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14. A probe card as claimed in claim 12,
20 wherein said decoupling capacitor is a thin-film
capacitor formed on a support substrate and has a
laminated structure formed on said support substrate,
said laminated structure including a dielectric film
sandwiched by upper and lower electrode films.

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15. A probe card for testing a semiconductor
30 chip, comprising:
a first interconnection substrate;
a second interconnection substrate mounted
on said first interconnection substrate such that
there is formed a gap between said first
35 interconnection substrate and said second
interconnection substrate; and
a plurality of probes provided on said

second interconnection substrate at a surface away
from said first interconnection substrate,
a difference of thermal expansion
coefficient between said first interconnection
5 substrate and said second interconnection substrate is
2ppm/°C or less.

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16. A probe card as claimed in claim 15,
wherein said second interconnection substrate has a
thermal expansion coefficient of 4 ± 2 ppm/°C.

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17. A probe card as claimed in claim 15,
wherein said second interconnection substrate carries,
20 on a surface thereof facing said first interconnection
substrate, a decoupling capacitor.

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18. A probe card as claimed in claim 15,
wherein said second interconnection substrate includes
an interconnection layer formed on a surface of any of
a resin-infiltrated carbon fiber board and an invar
30 board.

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19. A probe card as claimed in claim 15,
wherein said first interconnection substrate and said
second interconnection substrate are connected by a

pin grid array.

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20. A probe card as claimed in claim 15,
wherein said first interconnection substrate and said
second interconnection substrate are connected
detachably.

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21. A probe card as claimed in claim 15,
15 wherein said first interconnection substrate carries,
on a surface away from said second interconnection
substrate, a pin electronic module in a detachable
manner.

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22. A testing method of a semiconductor chip
by using a probe card,
25 said probe card comprising: a first
interconnection board; a second interconnection board
mounted on said first interconnection board in such a
manner that a gap is formed between said first
interconnection board and said second interconnection
30 board; a plurality of probes provided on said second
interconnection board at a surface away from said
first interconnection board; and a decoupling
capacitor provided on said second interconnection
board at a surface facing said first interconnection
35 board,

said method comprising the step, before
contacting said probe card to said semiconductor chip,

of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package including therein said semiconductor chip and a capacitor, for a part between
5 said semiconductor chip and said capacitor.

10 23. A testing method as claimed in claim 22, wherein said probe card has impedance between said probe and said decoupling capacitor set to fall within a range of -50% and +100% of the impedance of the semiconductor chip to be tested and a decoupling
15 capacitor connected to said semiconductor chip in a semiconductor device product.

20 24. A capacitor, comprising:
a dielectric film;
a first electrode film formed on a first principal surface of said dielectric film;
25 a second electrode film formed on a second principal surface of said dielectric film;
a first interconnection part extending from said first electrode film to a first side of a laminated structure formed of said dielectric film and
30 said first and second electrode films; and
a second interconnection part extending from said second electrode film to said first side,
a resin layer being formed on a second side of said laminated structure.

35 25. A capacitor as claimed in claim 24, wherein said capacitor carries another resin layer at

said first side of said laminated structure, said first interconnection part and said second interconnection part being exposed at a surface of said another resin layer.

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26. A capacitor as claimed in claim 24,
10 wherein said capacitor has a total thickness, defined as a thickness from a bottom surface of said resin layer to a top surface of said first and second interconnection parts, of $10\mu\text{m}$ or less.

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27. A capacitor as claimed in claim 24,
wherein said first and second interconnection parts
20 form respective contactors such that the contactors are aligned on a substantially flush plane.

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28. A capacitor as claimed in claim 24,
wherein said resin layer is selected from the group consisting of a polyimide resin, an epoxy resin, a bismaleimide triazine resin, a polytetrafluoroethylene
30 resin, a benzocyclobutene resin, an acryl resin, and diallyl phtalate resin.

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29. A capacitor as claimed in claim 24,
wherein said resin layer has a surface roughness of

5nm or less.

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30. A semiconductor device, comprising:
a capacitor; and
a semiconductor chip on which said capacitor
is mounted;

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said capacitor comprising: a dielectric
film; a first electrode film formed on a first
principal surface of said dielectric film; a second
electrode film formed on a second principal surface of
said dielectric film; a first interconnection part
15 extending from said first electrode film to a first
side of a laminated structure formed of said
dielectric film and said first and second electrode
films; and a second interconnection part extending
from said second electrode film to said first side, a
20 resin layer being formed on a second side of said
laminated structure.

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31. A method of manufacturing a capacitor,
comprising the steps of:

forming a first insulation film of a resin
30 on a substrate;
forming a first electrode film on said first
insulation film;
forming a dielectric film on said first
electrode film;
35 forming a second electrode film on said
dielectric film; and
removing said substrate by an etching

process such that said first insulation film is exposed.